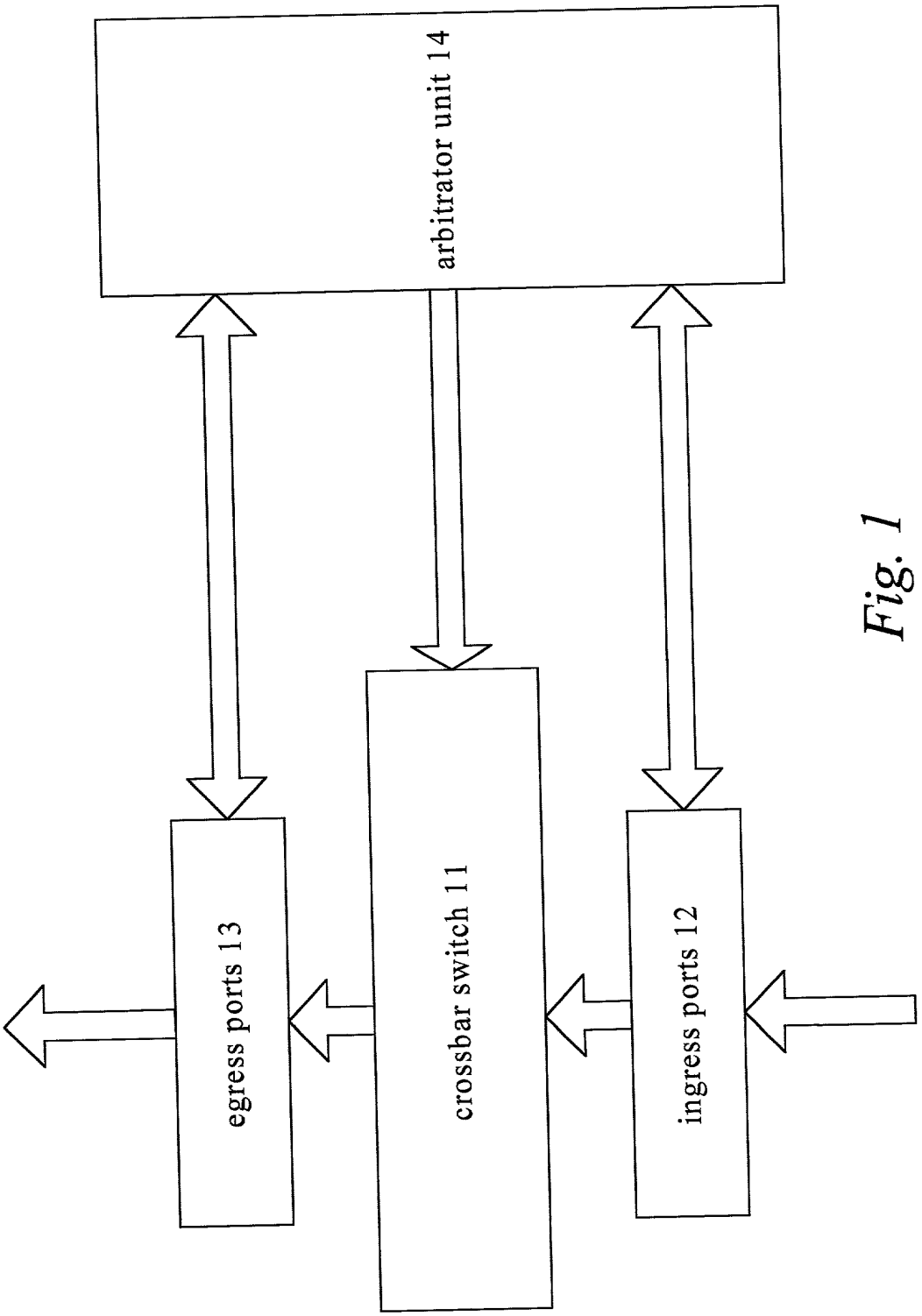
arbitrator unit 14
egress ports 13
crossbar switch 11
ingress ports 12

Fig. 1

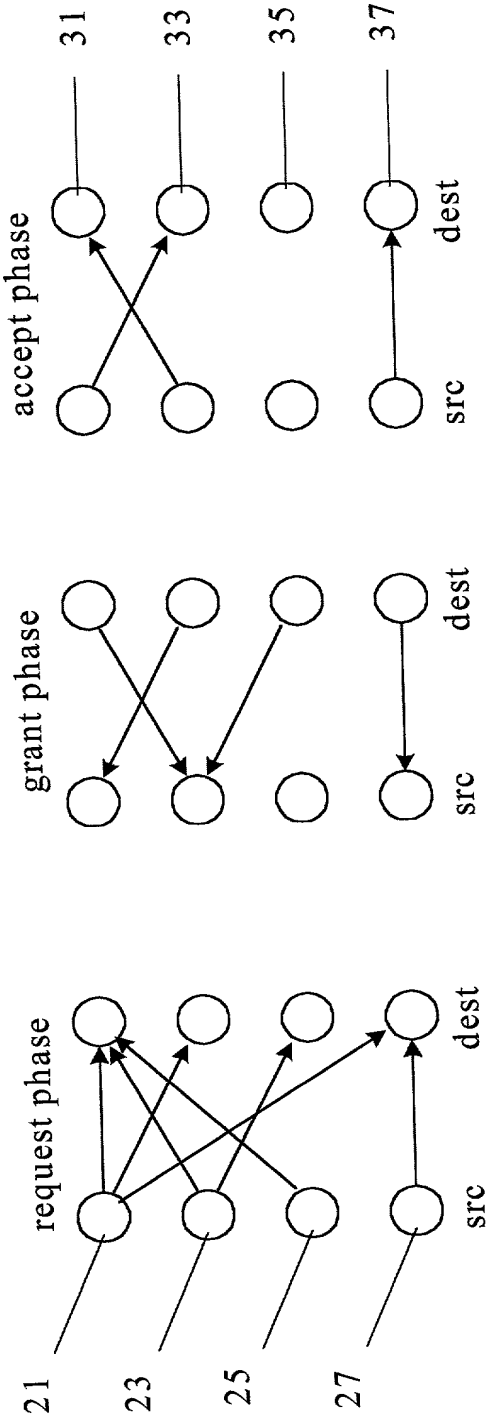
request phase
grant phase
accept phase
21
23
25
27
31
33
35
37
src
dest
src
dest
src
dest

Fig. 2

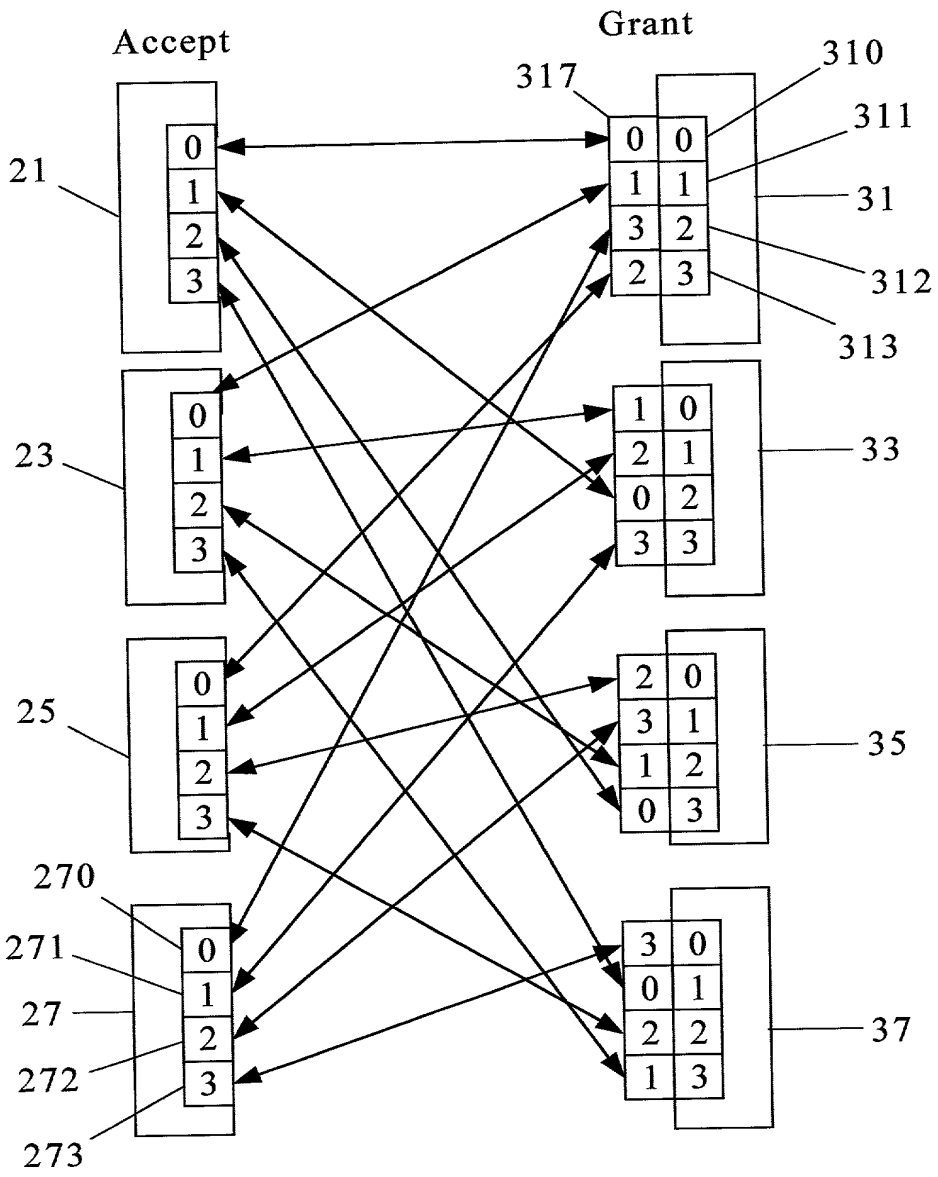
Accept
Grant
21
23
25
270
271
27
272
273
317
310
311
31
312
313
33
35
37

Fig. 3(a)

Original Pointer Value	Egress Port Number 0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	3	0	1	2
3	2	3	0	1

Mapped Pointer Value

Fig. 3(b)

M \ P	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	0	1	2	3	4	5	6	7
1	1	2	3	4	5	6	7	0
2	3	4	5	6	7	0	1	2
3	6	7	0	1	2	3	4	5
4	2	3	4	5	6	7	0	1
5	7	0	1	2	3	4	5	6
6	5	6	7	0	1	2	3	4
7	4	5	6	7	0	1	2	3

Fig. 4

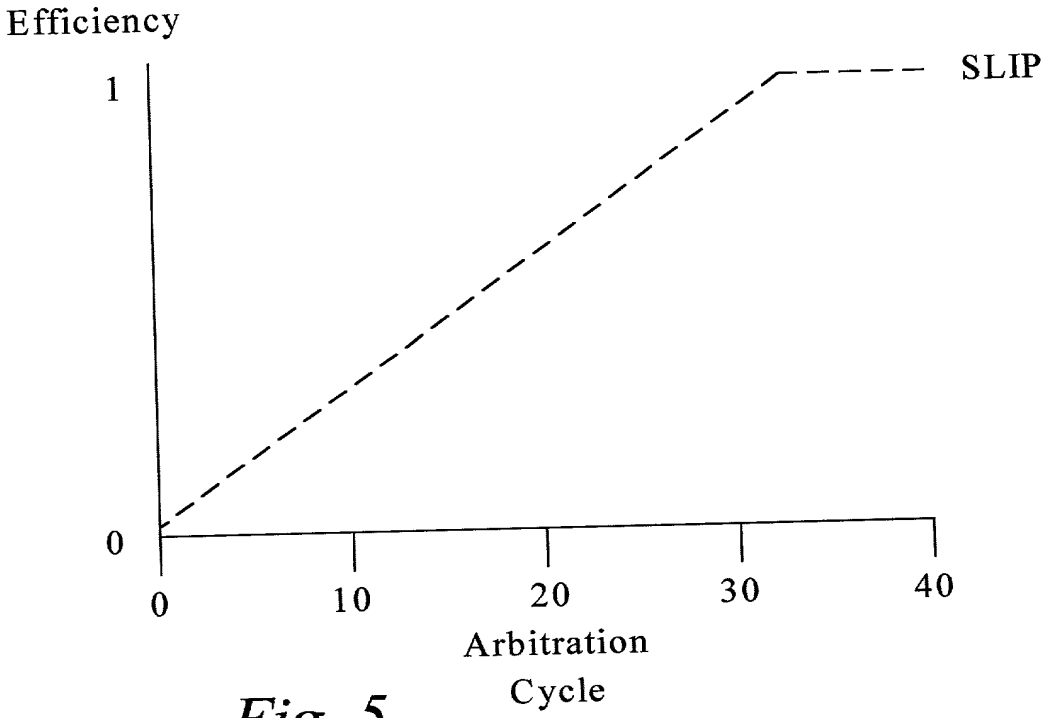

Fig. 5

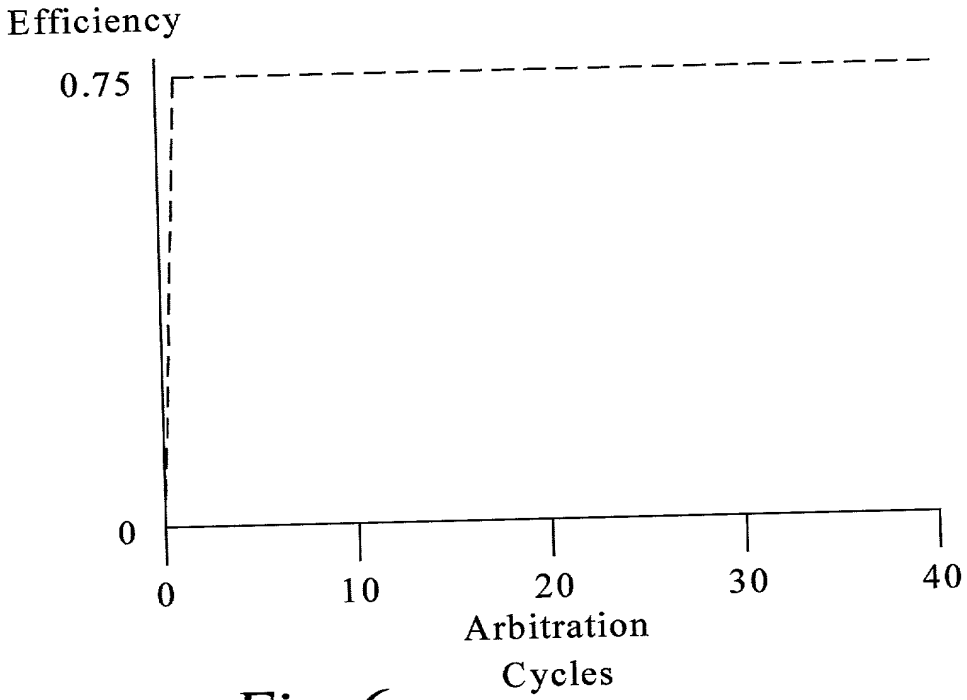

Fig. 6